**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A current supply control circuit for controlling an amount of current supplied to a differential circuit, comprising:

a bypass path for bypassing current around said differential circuit;

switching means, interposed in said bypath pass, for opening/closing said bypass path in accordance with a signal level of a clock signal ~~applied from the outside~~; and

control means for controlling the amount of current supplied to said differential circuit in accordance with the signal level of the clock signal ~~.~~;

said bypass path and said control means configured such that the amount of current supplied to said differential circuit is reduced in a case where said switching means closes said bypass path to cause current to flow through said bypass path.

2. (Original) The current supply control circuit according to claim 1, wherein said control means adjusts the amount of current in synchronization with opening/closing of said bypass path.

3. (Currently Amended) ~~The current supply control circuit according to claim 1, wherein:~~ A current supply control circuit for controlling an amount of current supplied to a differential circuit, comprising:

a bypass path for bypassing current around said differential circuit;

switching means, interposed in said bypath pass, for opening/closing said bypass path in accordance with a signal level of a clock signal applied from the outside; and

control means for controlling the amount of current supplied to said differential circuit in accordance with the signal level of the clock signal;

wherein said switching means has a current switching transistor, said current switching transistor having an emitter connected to a common emitter of said differential circuit, and

wherein said control means is connected to a connection point between the emitter of said current switching transistor and the common emitter of said differential circuit.

4. (Currently Amended) The current supply control circuit according to claim 3, wherein:

said control means has a current source transistor, said current source transistor having a collector connected to the connection point, and

said control means further comprises a feedback path for applying information about ~~the~~ a signal level at ~~the~~ a collector of said current switching transistor to a base of said current source transistor.

5. (Currently Amended) The current supply control circuit according to claim 3, wherein said control means comprises an output terminal for sending ~~the~~ information on ~~the~~ a signal level at ~~the~~ a collector of said current switching transistor to another logic circuit.

6. (Currently Amended) ~~The current supply control circuit according to claim 1,~~ A current supply control circuit for controlling an amount of current supplied to a differential circuit, comprising:

a bypass path for bypassing current around said differential circuit;

switching means, interposed in said bypath pass, for opening/closing said bypass path in accordance with a signal level of a clock signal applied from the outside; and

control means for controlling the amount of current supplied to said differential circuit in accordance with the signal level of the clock signal;

wherein said control means adjusts the current so that the amount of current supplied to said differential circuit when the signal level of the clock signal is at a low level is larger than the amount of current supplied to said differential circuit when the signal level of the clock signal is at a high level.

7. (Currently Amended) The current supply control circuit according to claim 3, wherein a parallel circuit comprising ~~of~~ a circuit element having an inductance component and a circuit element having a capacitance element is connected to ~~the~~ a collector of said current switching transistor.

8. (Currently Amended) The current supply control circuit according to claim 3, wherein a series circuit comprising ~~of~~ a circuit element having an inductance component with a circuit element having a capacitance component is connected to ~~the~~ a collector of said current switching transistor.

9. (Currently Amended) A latch circuit comprising:

a first differential circuit for reading a data signal ~~from the outside~~,

a second differential circuit for holding the data signal,

a first current supply control circuit for controlling an amount of current supplied to said first differential circuit, and

a second current supply control circuit for controlling ~~the~~ an amount of current supplied to said second differential circuit, ~~wherein:~~

wherein said first current supply control circuit comprises:

a first bypass path for bypassing current around said first differential circuit;

first switching means, interposed in said first bypass path, for opening/closing said first bypass path in accordance with a signal level of a clock signal ~~applied from the outside~~; and

first control means for controlling the amount of current supplied to said first differential circuit, ~~and~~

wherein said second current supply control circuit comprises:

a second bypass path for bypassing current around said second differential circuit;

second switching means, interposed in said second bypass path, for opening/closing said second bypass path in accordance with a signal level of a clock complementary signal ~~applied from the outside~~, said clock complementary signal having a signal level that is ~~the~~ an inverse of that of the clock signal; and

second control means for controlling the amount of current supplied to said second differential circuit, and

wherein ~~said first control means adjusts the amount of current in accordance with the signal level of the clock signal, and said second control means adjusts the amount of current~~

~~in accordance with the signal level of the clock complementary signal~~ said first bypass path and said first control means are configured such that the amount of current supplied to said first differential circuit is reduced in a case where said first switching means closes said first bypass path to cause current to flow through said first bypass path.

10. (Currently Amended) The latch circuit according to claim 9, wherein:

said first switching means has a first current switching transistor, said first current switching transistor having an emitter connected to a common emitter of said first differential circuit, ~~and~~

said first control means has a first current source transistor, said first current source transistor having a collector connected to the common emitter of said first differential circuit,

said second switching means has a second current switching transistor, said second current switching transistor having an emitter connected to a common emitter of said second differential circuit, ~~and~~

said second control means ~~having~~ has a second current source transistor, said second current source transistor having a collector connected to the common emitter of said second differential circuit,

said first current switching transistor has a base connected to a base of said second current source transistor through a first level shift circuit, and

said second current switching transistor has a base connected to the base of said first current source transistor through a second level shift circuit.

11. (Currently Amended) The latch circuit according to claim 9, wherein said first control means adjusts the amount of current supplied to said first differential circuit in accordance with the signal level of the clock signal, and said second control means adjusts the amount of current supplied to said second differential circuit in accordance with the signal level of the clock complementary signal. ~~said first and second current supply control circuits are current supply control circuits comprising:~~

~~a bypass path for bypassing current around said differential circuit;~~

~~switching means, interposed in said bypath pass, for opening/closing said bypass path in accordance with a signal level of a clock signal applied from the outside; and~~

~~control means for controlling the amount of current supplied to said differential circuit in accordance with the signal level of the clock signal.~~

12. (Currently Amended) A selector circuit comprising:

a first differential circuit for reading a first data signal ~~from an outside~~,

a second differential circuit for reading a second data signal ~~from the outside~~,

a first current supply control circuit for controlling an amount of current supplied to said first differential circuit, and

a second current supply control circuit for controlling ~~the~~ an amount of current supplied to said second differential circuit, ~~wherein:~~

wherein said first current supply control circuit comprises:

a first bypass path for bypassing current around said first differential circuit;

first switching means, interposed in said first bypass path, for opening/closing said first bypass path in accordance with a signal level of a clock signal ~~applied thereto from the outside~~; and

first control means for controlling the amount of current supplied to said first differential circuit, ~~and~~

wherein said second current supply control circuit comprises:

a second bypass path for bypassing current around said second differential circuit;

second switching means, interposed in said second bypass path, for opening/closing said second bypass path in accordance with a signal level of a clock complementary signal ~~applied from the outside~~, said clock complementary signal having a signal level that is ~~the~~ an inverse of that of the clock signal; and

second control means for controlling the amount of current supplied to said second differential circuit,

wherein ~~said first control means adjusts the amount of current in accordance with the signal level of the clock signal, said second control means adjusts the amount of current in accordance with the signal level of the complementary clock signal, and said selector circuit alternately delivers the first data signal and the second data signal~~ said first bypass path and said first control means are configured such that the amount of current supplied to said first

differential circuit is reduced in a case where said first switching means closes said first bypass path to cause current to flow through said first bypass path.

13. (Currently Amended) The selector circuit according to claim 12, wherein:

said first switching means has s first current switching transistor, said first current switching transistor having an emitter connected to a common emitter of said first differential circuit, ~~and~~

said first control means has a first current source transistor, said first current source transistor having a collector connected to the common emitter of said first differential circuit,

said second switching means has a second current switching transistor, said second current switching transistor having an emitter connected to a common emitter of said second differential circuit, ~~and~~

said second control means has a second current source transistor, said second current source transistor having a collector connected to the common emitter of said second differential circuit,

said first current switching transistor has a base connected to a base of said second current source transistor through a first level shift circuit, and

said second current switching transistor has a base connected to a base of said first current source transistor through a second level shift circuit.

14. (Currently Amended) The selector circuit according to claim 12, wherein said first control means adjusts the amount of current supplied to said first differential circuit in accordance with the signal level of the clock signal, said second control means adjusts the amount of current supplied to said second differential circuit in accordance with the signal level of the clock complementary signal. ~~said first and second current supply control circuits are current supply control circuits comprising:~~

~~a bypass path for bypassing current around said differential circuit;~~

~~switching means, interposed in said bypath pass, for opening/closing said bypass path in accordance with a signal level of a clock signal applied from the outside; and~~

~~control means for controlling the amount of current supplied to said differential circuit in accordance with the signal level of the clock signal~~.

15. (Currently Amended) A circuit block comprising:

a current supply control circuit comprising:

a bypass path for bypassing current around ~~said~~ a differential circuit;

switching means, interposed in said bypath pass, for opening/closing said bypass path in accordance with a signal level of a clock signal applied from the outside; and

control means for controlling ~~the~~ an amount of current supplied to said differential circuit in accordance with the signal level of the clock signal; and

a first and a second logic circuit for processing a data signal applied from the outside in synchronization with a change in signal level of a corresponding clock signal,

wherein:

said switching means has a current switching transistor, said current switching transistor having an emitter connected to a common emitter of said differential circuit, and

said control means is connected to a connection point between the emitter of said current switching transistor and the common emitter of said differential circuit,

wherein said control means comprises an output terminal for sending ~~the~~ information on ~~the~~ a signal level at ~~the~~ a collector of said current switching transistor to another logic circuit, and

wherein said first logic circuit delivers the information about ~~a~~ the signal level at ~~a~~ the collector of ~~a~~ the current switching transistor included in said current supply control circuit to said second logic circuit as ~~a~~ the clock signal corresponding to the second logic circuit.

16. (Currently Amended) The current supply control circuit according to claim 2, wherein:

said switching means has a current switching transistor, said current switching transistor having an emitter connected to a common emitter of said differential circuit, and

said control means is connected to a connection point between the emitter of said current switching transistor and the common emitter of said differential circuit.

17. (Currently Amended) The current supply control circuit according to claim ~~3~~ 16, wherein a parallel circuit comprising ~~of~~ a circuit element having an inductance component and a

circuit element having a capacitance element is connected to ~~the~~ a collector of said current switching transistor.

18. (Currently Amended) The current supply control circuit according to claim 4, wherein a parallel circuit comprising ~~of~~ a circuit element having an inductance component and a circuit element having a capacitance element is connected to ~~the~~ a collector of said current switching transistor.

19. (Currently Amended) The current supply control circuit according to claim 5, wherein a parallel circuit comprising ~~of~~ a circuit element having an inductance component and a circuit element having a capacitance element is connected to ~~the~~ a collector of said current switching transistor.

20. – 21. (Cancelled)

22. (Currently Amended) The current supply control circuit according to claim 6, wherein a parallel circuit comprising ~~of~~ a circuit element having an inductance component and a circuit element having a capacitance element is connected to ~~the collector of said current switching transistor~~ said switching means.

23. (Currently Amended) The current supply control circuit according to claim 4, wherein a series circuit comprising ~~of~~ a circuit element having an inductance component with a circuit element having a capacitance component is connected to ~~the~~ a collector of said current switching transistor.

24. (Currently Amended) The current supply control circuit according to claim 5, wherein a series circuit comprising ~~of~~ a circuit element having an inductance component with a circuit element having a capacitance component is connected to ~~the~~ a collector of said current switching transistor.

25. (Currently Amended) The current supply control circuit according to claim 6, wherein a series circuit comprising ~~of~~ a circuit element having an inductance component with a circuit element having a capacitance component is connected to ~~the collector of said current switching transistor~~ said switching means.

26. (New) The current supply control circuit according to claim 16, wherein a series circuit comprising a circuit element having an inductance component with a circuit element having a capacitance component is connected to a collector of said current switching transistor.

27. (New) The current supply control circuit according to claim 1, wherein said bypass path is directly connected to a common emitter of said differential circuit.